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**United States Patent** [19]**Ball**

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**[54] MULTI-CHIP STACKED DEVICES****[75] Inventor:** Michael B. Ball, Boise, Id.**[73] Assignee:** Micron Semiconductor, Inc., Boise, Id.**[21] Appl. No.:** 43,503**[22] Filed:** Apr. 6, 1993**[51] Int. Cl.<sup>3</sup>** ..... H01L 23/48; H01L 29/40;  
H01L 23/02; H01L 23/32**[52] U.S. Cl.** ..... 257/686; 257/686;  
257/782; 257/783; 257/676**[58] Field of Search** ..... 257/777, 782, 783, 676,  
257/686**[56] References Cited****U.S. PATENT DOCUMENTS**

4,567,643 2/1986 Droguet et al. .... 29/575  
 4,984,059 1/1991 Kubota et al. .... 357/68  
 4,996,587 2/1991 Hinrichsmeyer et al. .... 357/74  
 5,012,323 4/1991 Farnworth ..... 357/75  
 5,049,976 9/1991 Demmin et al. .... 357/71

**FOREIGN PATENT DOCUMENTS**

56-62351A 5/1981 Japan ..... H01L 25/04  
 60-182731 9/1985 Japan ..... 257/777  
 62-126661 6/1987 Japan ..... 257/686  
 1-28856 1/1989 Japan  
 3-169062 7/1991 Japan ..... 257/686

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Springer & Hoopes**[57] ABSTRACT**

A multiple stacked die device is disclosed that contains up to four dies and does not exceed the height of current single die packages. Close-tolerance stacking is made possible by a low-loop-profile wire-bonding operation and thin-adhesive layer between the stacked dies.

**2 Claims, 2 Drawing Sheets**

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